



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

JSFw

Ashik Kumar Shivacharya Nagaraj et al.

Title:
COMPILER

COMBINATIONAL APPROACH FOR DEVELOPING BUILDING BLOCKS OF DSP

Docket No.: 884.891US1
Filed: September 30, 2003
Examiner: Unknown

Serial No.: 10/675,910
Due Date: N/A
Group Art Unit: 2183

MS Amendment

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ Return postcard.
- ☒ Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), and copies of 7 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer Number 21186

By: *Ann M. McCrackin*
Atty: Ann M. McCrackin
Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 30th day of June, 2006.

JAMES KANYOSIK
Name

James Kanyosik
Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)



10/675,910

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ashik Kumar Shivacharya Nagaraj et al.	Examiner:	Unknown
Serial No.:	10/675,910	Group Art Unit:	2183
Filed:	September 30, 2003	Docket:	884.891US1
Title:	COMBINATIONAL APPROACH FOR DEVELOPING BUILDING BLOCKS OF DSP COMPILER		
Assignee:	Intel Corporation	Customer Number:	21186

INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

INFORMATION DISCLOSURE STATEMENT

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Customer No.: 21186

Dkt: 884.891US1 (INTEL)

Serial No.: 10/675,910

Filing Date: September 30, 2003

Title: COMBINATIONAL APPROACH FOR DEVELOPING BUILDING BLOCKS OF DSP COMPILER

Assignee: Intel Corporation

Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

ASHIK KUMAR SHIVACHARYA NAGARAJ ET AL.

By their Representatives,

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Date June 30, 2006

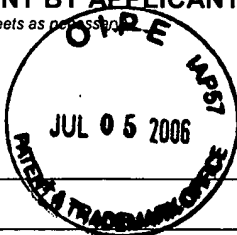
By Ann M. McCracklin
Ann M. McCracklin
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 30th day of June 2006.

JAMES KAUCSIK
Name

[Signature]
Signature

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)



Complete if Known

Application Number	10/675,910
Filing Date	September 30, 2003
First Named Inventor	Nagaraj, Ashik Kumar
Group Art Unit	2183
Examiner Name	Unknown

Sheet 1 of 1

Attorney Docket No: 884.891US1

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		"AC/DC Project", http://web.archive.org/web/20030814011852/www.daimi.au.dk/CPnets/ACDC/ , (archived August 14, 2003), 2 pgs.	
		"HP Labs 2001 Technical Reports Abstracts", http://web.archive.org/web/20021214001120/http://www.hpl.hp.com/techreports/2001/ , (archived December 14, 2002), 9 pgs.	
		"Xerox Finite-State Compiler", http://web.archive.org/web/20020202050301/http://www.xrce.xerox.com/research/mlttfst , (archived February 2, 2002), 1 pg.	
		LORENZ, M., et al., "Energy Aware Compilation for DSPs with SIMD Instructions", <u>LCTES '02 - SCOPES '02</u> , (2002), 8 pgs.	
		LORENZ, M., et al., "Low-Energy DSP Code Generation Using a Genetic Algorithm", <u>Proceedings of the International Conference on Computer Design: VLSI in Computers & Processors (ICCD '01)</u> , (2001), 7 pgs.	
		LORENZ, M., et al., "Optimized Address Assignment for DSPs With SIMD Memory Accesses", <u>Proceedings of the 2001 Conference on Asia South Pacific Design Automation</u> , (2001), 415-420	
		WEISS, M. H., et al., "Toolumgebung fur plattformbasierte DSPs der nachsten Generation", <u>Conference Proceedings, DSP Deutschland</u> , (1999), 10 pgs.	

EXAMINER

DATE CONSIDERED